



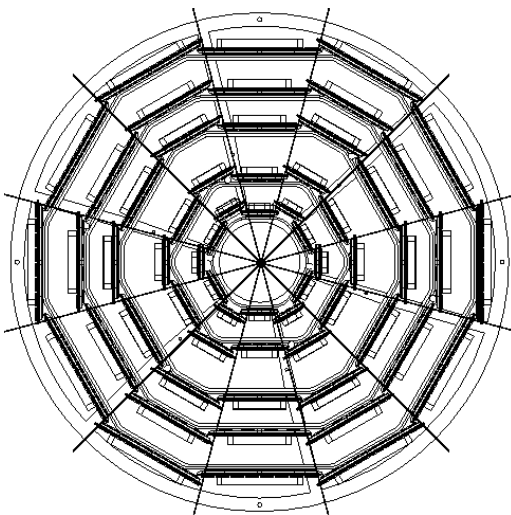
# SVT Changes for SVX 2b Geometry

- Two of SVT's design assumptions no longer hold for Run 2B silicon detector

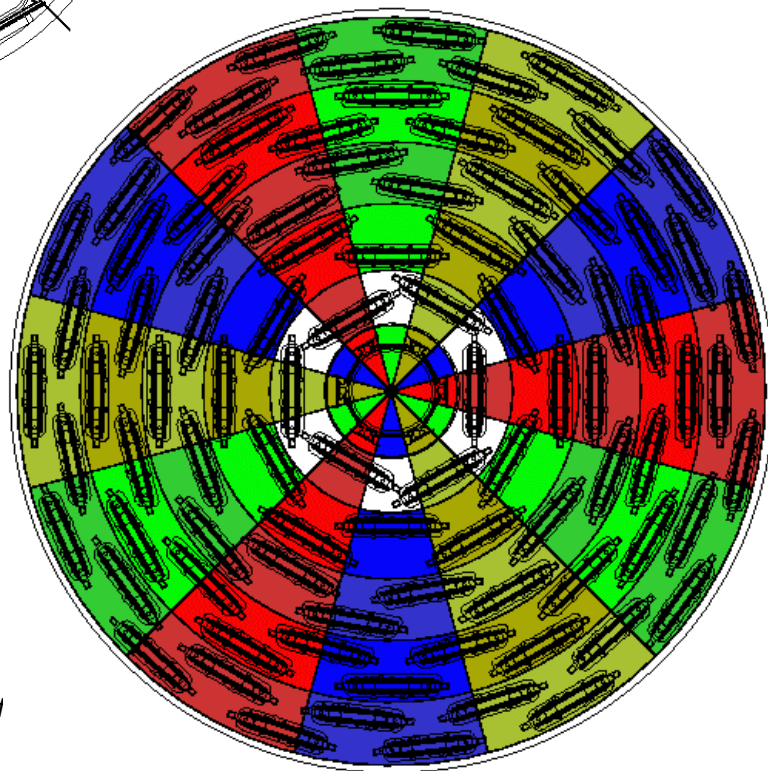
- ➔ Perfect 12-fold “wedge” symmetry
- ➔ Measurement layers whose radii can be approximated as constant within a wedge

- Can be addressed with minor modifications

- ➔ Add 12 Merger boards
  - ➔ produce additional boards from existing design
- ➔ Upgrade Fitter boards
  - ➔ extend current design



Run 2A geometry

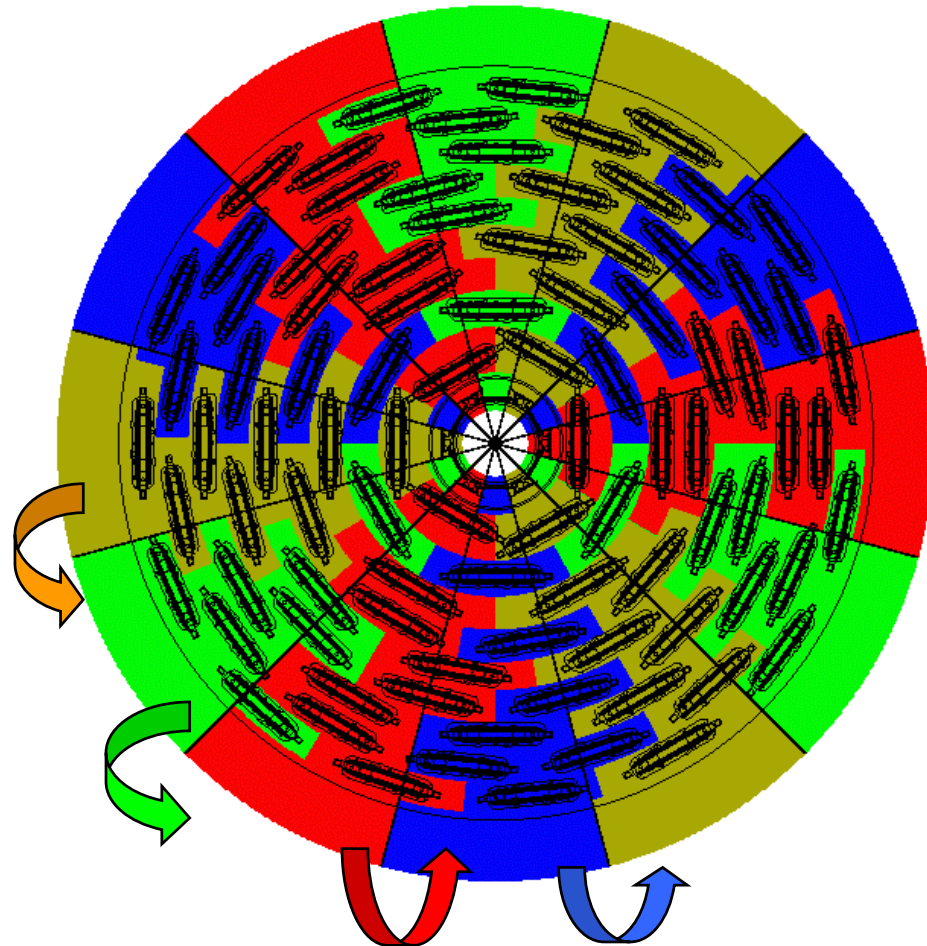


Run 2B geometry



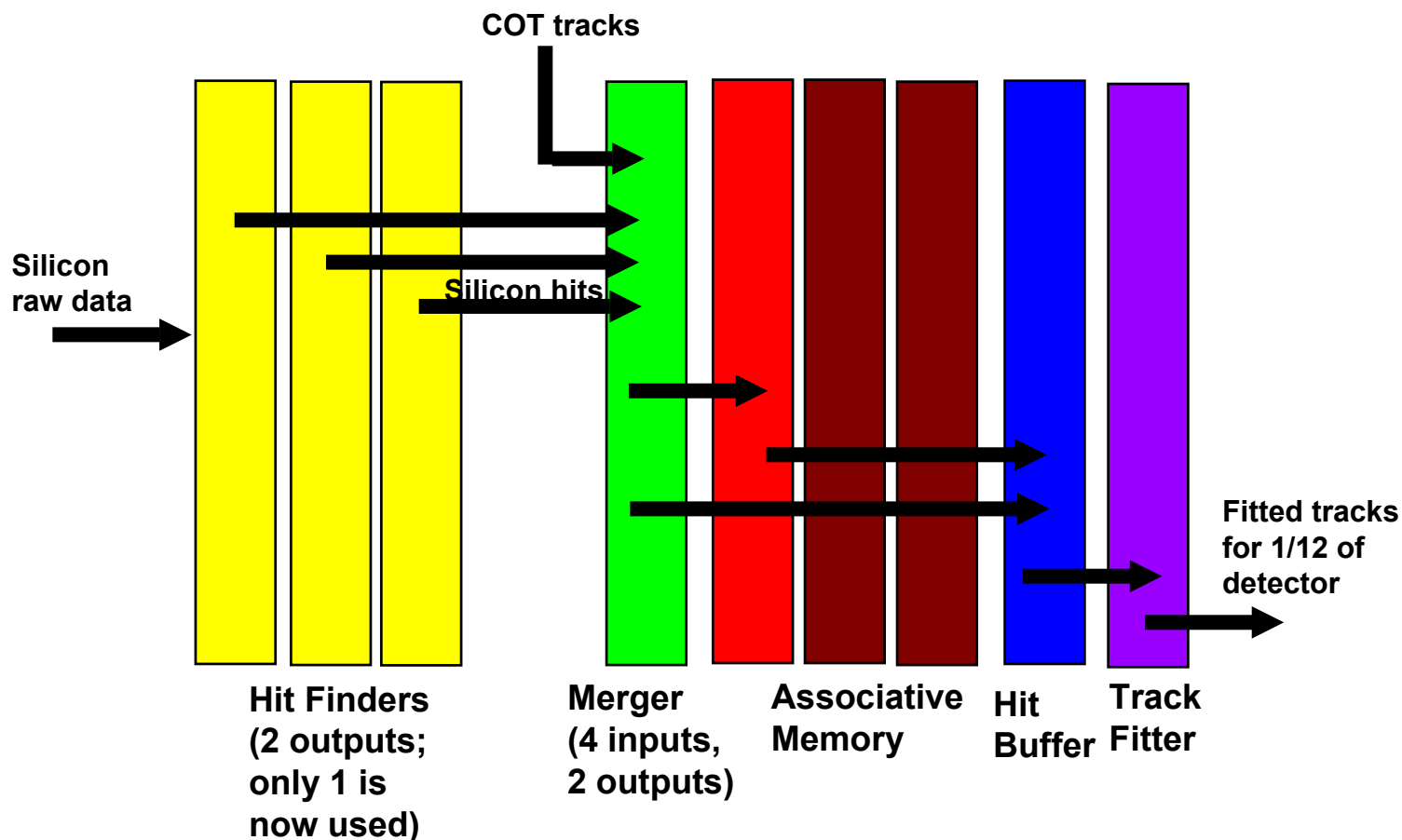
# Recovering “wedge” geometry for SVT

- SVT is built as 12 identical units, finding/fitting tracks in parallel
  - ➔ 1/12 of SVT processes 1/12 of detector in azimuth
- In upgraded detector, some staves in outer layers span SVT wedge boundaries
  - ➔ These staves' hit data must be split among two SVT wedges
  - ➔ Detector will be cabled such that data only feed forward in azimuth, never backward
    - ➔ Detector data received by Hit Finders in SVT wedge N can be used for tracking in SVT wedges N & N+1
  - ➔ SVT wedge N receives some hits from wedge N-1, forwards some hits to wedge N+1



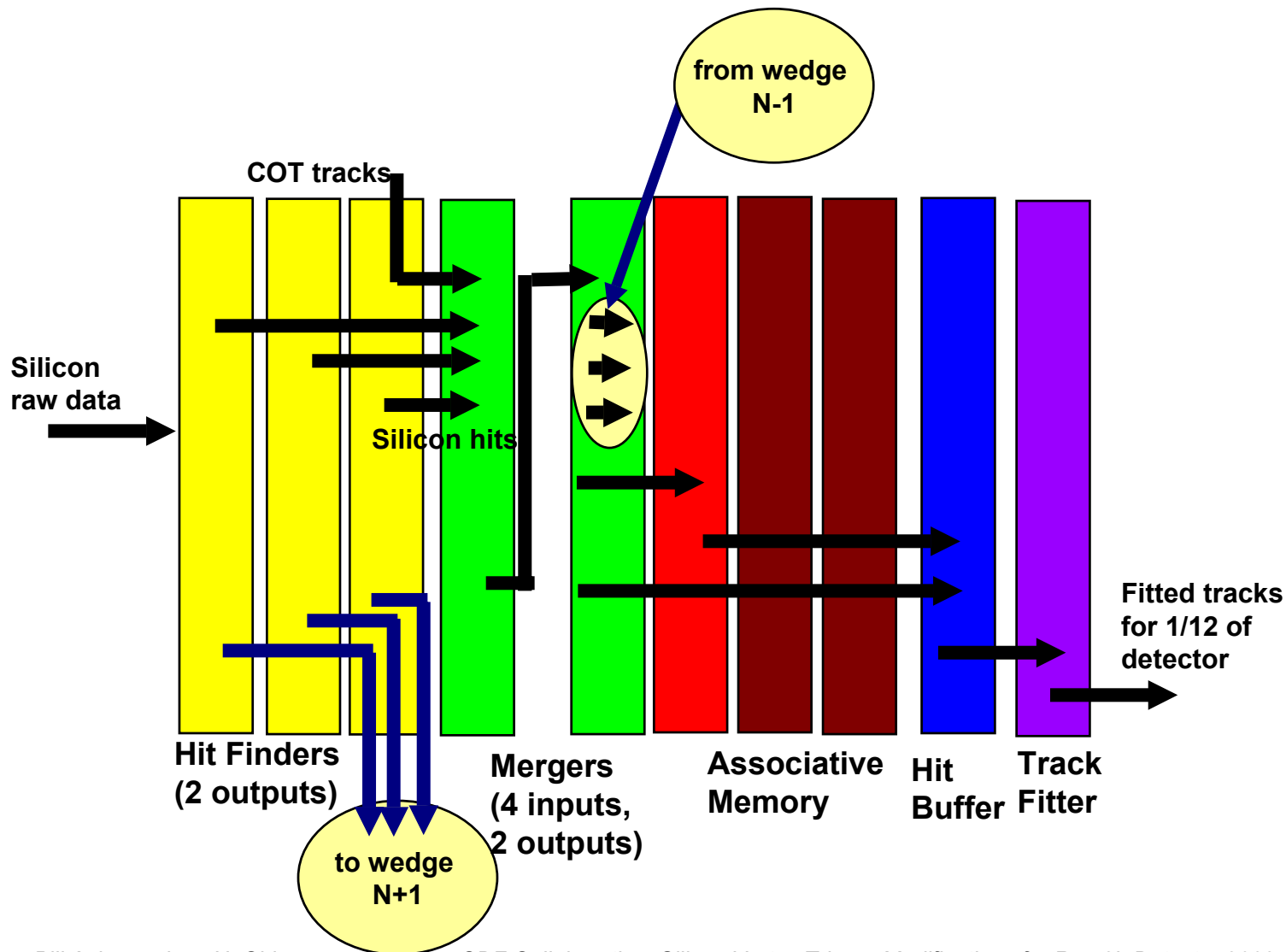


# Run 2a SVT data flow (per wedge)





# Run 2b SVT data flow (per wedge)





# SVT Track Fitter Changes for SVX 2b Geometry

- SVT TF performs fast, linearized fit in FPGAs
  - ➔ 6 measurements  $\rightarrow$  3 parameters plus  $\chi^2$ 
    - ➔  $(c, \phi, d, \chi_1, \chi_2, \chi_3) = \vec{p} = \vec{p}_0 + V \cdot \vec{x}$
  - ➔ Uses road ID to reduce bits in multiply
    - ➔  $\vec{p} = \vec{p}_0^{\text{road}} + V \cdot (\vec{x} - \vec{x}^{\text{road}})$
  - ➔ 250 nsec per track fit!
- For a given set of layers, coefficients are constant across a wedge
- To handle stave geometry, fit coefficients for a given layer combination must vary within an SVT wedge
  - ➔ In present Track Fitters, coefficients are stored in FPGA internal SRAM
    - ➔ 70% of RAM, 60% of logic is used in FIT chip
  - ➔ Number of sets of coefficients needed per Track Fitter will increase by an order of magnitude
  - ➔ Newer FPGAs can meet this need, without any fundamental TF design change

